ENGLISH TRANSLATION OF
TAIWAN PATENT NO. 177,766

Method for Fan Out Type Wafer Level Package

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a package for semiconductors, and more particularly to a fan out type wafer level package.

2. Description of the Prior Art

The integrated circuit technologies are developing very fast, and especially electrical elements have a tendency toward miniaturization. The needs of more and more different electrical elements and applications are following by the development of computer and communication technology. F or example, more memory elements and different type semiconductor elements are necessary for working with voice interfaces of computers or other communication interfaces. How ever, the integrated circuit technology tends to higher intensity. With the development of semiconductor technology and the electrical products under the urgent requirements of light and functional, the IC semiconductor has higher intensity I/O numbers, so that the contact numbers of the package elements are more and more numerous and rapid. The semiconductor chip is usually individually packaged in plastic or ceramic materials. The main purpose of the package structure is to protect the dies from outside damages. Furthermore, the heat generated by the dies must be diffused efficiently through the package structure to ensure the operation the dies.

In earlier package technology focused on lead frame, the pins are used to input and output signals. The earlier lead frame package technology is already not suitable for the advanced semiconductor dies due to the density of the pins thereof is too high. Hence, a new package technology of BGA (Ball Grid Array) has been developed to satisfy the packaging requirement for the advanced semiconductor dies. The BGA

package has an advantage of that the spherical pins has a shorter pitch than that of the lead frame package and the pins is hard to damage and deform. In addition, the shorter signal transmitting distance benefits to raise the operating frequency to conform to the requirement of faster efficiency. For example, the U.S. patent No. 5,629,835 discloses a BGA package, by Mahulikar et al; the U.S. patent No. 5,239,198 discloses another package that the FR4 substrates having a pattern of conductive traces thereon are mounted on a PCB.

Most of the package technologies divide dies on a wafer into respective dies and then to package and test the die respectively. Another package technology, called "Wafer Level Package (WLP)", can package the dies on a wafer before dividing the dies into respective dies. The WLP technology has some advantages, such as a shorter producing cycle time, lower cost, and no need to under-fill or molding. The U.S. patent No. 5,323,051, "Semiconductor wafer level package", is disclosed a WLP technology by Adams et al. The technology is described as follow. A die is formed on a surface of a semiconductor wafer, and a cap wafer with a predetermined pattern of frit glass walls as a bonding agent is deposited on a surface of the semiconductor wafer, such that the die is completely surrounded by the frit glass walls. Then, a surface of the semiconductor wafer without the die is polished to reduce the height of the semiconductor wafer; the process is generally called "Back Grinding". Next, the dice are etched to separate IC and exposed portion of glue material.

Besides, the size of the die is very small, and the I/O pads are formed on a surface of a die in the conventional arts. Furthermore, the number of the pads is limited due to the dice area and a too short pitch among pads results in a problem of signal coupling or signal interference.

Because of the predominant tendency of wafer level package, the characteristic of the present invention is to replace the I/O bumping positions on the surface of dice by a fan out type process, and extend the contact points to improve the larger area for bumping of I/O bumping. Therefore, the advantage is to increase the I/O bumping numbers, namely to increase more I/O, or maintain the shortest pitch to avoid the

problems of the signal coupling due to the too closer dice and signal interference due to the too closer solder contacts.

SUMMARY OF THE INVENTION

Therefore, the present invention has been made in view of the above problems in the prior arts, and it is an objective of the present invention to provide a process for fan out type wafer level package.

Another objective of the present invention is to provide a fan out type wafer level package and the process for the same.

The present invention provides a process for a fan out type wafer level package comprising providing a sawed wafer after selecting, picking good dice, and sucking and placing to rearrange on a new glass base. Each die is attached on the base by adhesion. The dice are placed on the glass base to extend the pitch between the dice in order to have more space to accumulate the fan out type ball array in following process. The fan out type package technology can improve the I/O numbers or maintain the appropriate pitch between the dice to avoid the signal interference by the shorten size of the dice. The surface of the packaging wafer (or the first surface) has the input/output metal pad, such as the aluminum pad. The metal pad is used for inter connection, and formed on the wafer by the alignment of mask, exposure and development. A BCB (Benzocyclobutene) isolating layer is coating on the wafer and the aluminum pad by spin coater, and then a Ni/Au-containing film formed on the surface of the aluminum pad. Then, the dice are sawed to form individual die. The processed dice are placed on the glass base with adhesion by using the sucking and placing machine, and the dice are cured.

Next, a first epoxy layer is filled on the isolating base, the dice, the BCB and the aluminum pad of the first opening. Then, the first epoxy layer is removed by photo resist type etching or chemical reagent to expose the second opening, and the first epoxy layer is cured in the oven. The solder is filled to the second opening by a

printing method.

Then, Ti/Cu film is coated on the solder, and a portion of the copper conductive line formed on Ti/Cu film is plated by a fan out process. One end of the copper conductive line is aligned with the aluminum pad, and another end of the copper conductive line is introduced in fan out type. Before defining the remove the photo resist of the copper conductive line, a Ni/Au-containing film is plated, and then the photo resist is removed and the Ti/Cu film is etched. A second epoxy layer is coating on the copper conductive line and the bottom epoxy, and the second epoxy layer is cured by UV curing or heating curing.

Next, a portion of the second epoxy layer formed on the copper conductive line is removed to form the third opening, and its position is as possible as placed at the exterior side (far from the one side of the aluminum pad) of the copper conductive line for the fan out type I/O structure.

A Ni film is formed on the third opening and then the solder balls are bumped at the third opening and on the Ni film by a printing method or a bumping process. The position of the solder balls is not on the upper portion of the metal pad, but is horizontally and laterally extended to the lateral side of the metal pad. Finally, the solder balls and the glass base are sawed.

The present invention also provides a fan out type package structure. The package structure comprises an isolating base; a die adhered on the isolating base, wherein the wafer includes pluralities of aluminum pad formed thereon; a BCB layer coated on the surface of the dice and having pluralities of the first opening exposed to pluralities of the aluminum pad; solder filled to the first opening; a first epoxy layer coating on the dice, the isolating base and the BCB layer; conductive lines placed to the first epoxy layer and connected with the solder; a second epoxy layer coated on the copper conductive lines and having a second opening exposed a portion of the conductive lines; and solder balls placed on the second epoxy layer and filling to the second opening and connected with the copper conductive lines.

The package structure further comprises a copper seed layer formed on the first solder, and the copper seed layer includes Ti/Cu or Ni/Cu. The package structure further comprises a barrier or glue layer formed on the aluminum pad, and the material of the barrier or glue layer includes Ni/Au. The interface between the solder ball and copper conductive lines includes Ni. The package structure of the present invention is called ACE BGA (the Ball Grid Array of the Advanced Chip Engineering Technology Inc.).

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic diagram of a wafer level package placed on the glass base after sawing a single die from a wafer;

FIG. 2 is a schematic diagram of a wafer level package having dice with capacitor placed on the glass base after sawing from a wafer;

FIG. 3 is a schematic diagram of a BCB (Benzocyclobutene) protective layer formed on the surface of the dice having the metal pad;

FIG. 4 is a schematic diagram of removing a portion of BCB protective layer according to the present invention;

FIG. 5 is a schematic diagram of the dice attached to the base after sucking and placing according to the present invention;

FIG. 6 is a schematic diagram of filling a first epoxy layer according to the

present invention;

FIG. 7 is a schematic diagram of removing the first epoxy layer above the aluminum pad by a photo resist type etching or chemical reagent according to the present invention;

FIG. 8 is a schematic diagram of filling solder to the second opening by a printing process according to the present invention;

FIG. 9 is a schematic diagram of plating a portion of the copper conductive lines by alignment, exposure and developer according to the present invention;

FIG. 10 is a schematic diagram of coating a second epoxy layer according to the present invention;

FIG. 11 is a schematic diagram of removing the upper portion of the second epoxy layer on the copper conductive lines and forming the third opening according to the present invention;

FIG. 12 is a schematic diagram of bumping the solder balls by a printing process or a bumping process according to the present invention;

FIG. 13 is a schematic diagram of sawing line between sawing the dice and dice and glass base according to the present invention;

FIG. 14 is a schematic diagram of related positions of various barrier layers on the dice according to the present invention;

FIG. 15 is a cross-section diagram of single die of fan out type wafer level package according to the present invention;

FIG. 16 is a cross-section diagram of bumping the capacitor on the glass base

and single die of fan out type wafer level package according to the present invention; and

FIG. 17 is a cross-section diagram of a fan out type wafer level package in the process for multi dice package according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Some sample embodiments of the invention will now be described in greater detail. Nevertheless, it should be recognized that the present invention can be practiced in a wide range of other embodiments besides those explicitly described, and the scope of the present invention is expressly not limited expect as specified in the accompanying claims.

Then, the components of the different elements are not shown to scale. Some dimensions of the related components are exaggerated and meaningless portions are not drawn to provide a more clear description and comprehension of the present invention.

The essence of the present invention is to pick and place standard dies on a new base for obtaining an appropriate and wider distance between dies than the original distance of dies on a wafer. Therefore, the package structure has a larger size of balls array than the size of the die to avoid the problem of having too close ball pitch. Moreover, the die may be packaged with passive components (ex. capacitors) or other dies with a side by side structure or a stacking structure. The detailed process of the present invention will be described below.

Refer to Fig. 1, the divided dies are tested to choose standard good dies there from. The standard good dies are picked and replaced onto a new base 1 (the base is glass, ceramic or silicon crystal), and individual dice are adhered to the base 1. The thickness of the glue layer is approximately 10 μm. The adhesion is used by the spin

coater during curing process. The dice are placed on the glass base, and the pitch between the dice is extended in order to have a sufficient space to receive the fan out type ball array. The fan out process can increase the I/O numbers or maintain the appropriate pitch to avoid the problems of the signal interference. The package area is determined by the pitch between the following fan out type ball array. In another embodiment, the glass base further comprises the capacitor 1b placed on the lateral side of the dice to improve the efficiency of the filter, as shown in FIG. 2.

The package process is described as follows. Refer to Fig. 3, the surface of the packaging wafer (or the first surface) is used to as the input/output metal pad, such as the aluminum pad 4. The metal pad is used for inter connection, and formed on the wafer by the alignment of mask, exposure and development. A BCB (Benzocyclobutene) isolating layer 8 on the wafer is coated on the dice 2 and the aluminum pad 4 by spin coater to protect the dice. The thickness of the BCB isolating layer is approximately 5-10 μ m.

Next, a portion of the BCB layer 8 is removed by the alignment of mask, exposure and development process to form a first opening 9, and to expose the metal aluminum pad 4. It is noted that the scribe line is exposed and the dimension of opening is larger than the width of the scribe line to avoid the damage to the BCB layer during sawing, as shown in Fig. 4. Then, a Ni/Au-containing film is formed on the aluminum pad 4 by electroplating.

After sawing, as shown in Fig. 5, the pluralities of the dice 2a (the wafer is processed to form the dice by sawing) after tested and chosen are placed on the glass base 6 by the sucking and placing machine. The dice 2a are adhered on the glass base 5 by the glue reagent 7, and then the dice 2a are cured in an oven.

A first epoxy layer 10 is filled on the glass base 6, the dice 2a, the BCB layer 8 and the upper portion of the aluminum pad 4. Next, the first epoxy layer 10 on the aluminum pad 4 is removed by photo resist type etching or chemical reagent to form the second opening 13, and the aluminum pad 4 is exposed. The first epoxy layer 10

is cured in an oven and the thickness of the first epoxy layer 10 is approximately between 10-25 μ m (the thickness refers the thickness on the dice surface).

Next, the remaining epoxy layer 10 is cleaned by a RIE plasma process, and the remaining epoxy layer 10 is defined as 10. The Ni/Au film or Ni-containing film 11 is used as a barrier or glue layer.

The second opening 13 above the Ni/Au or Ni-containing film 11 is filled with solder 12 by a printing method. The solder 12 is cured by the IR reflow process. Then, a Ti/Cu film 19 is sputtered on the remaining epoxy layer 10 and the solder 12, as shown in Fig. 8, to act as seeding layer.

Refer to Fig. 9, the copper pattern is defined by the photo resist (not shown), and the copper conductive lines is formed on the Ti/Cu film 19 by electroplating process. One end of the copper conductive line 14 is aligned to the internal side (internal side of the dice) of the solder 12 of the second opening, and another end of the copper conductive line is introduced in fan out type. Namely, on end of the position of the copper conductive line 14 is aligned with the aluminum pad 4, and other end of the copper conductive line 14 is introduced in fan out type. The interface between the conductive line 14 and the lower epoxy layer 10, solder 12 is larger than the opening of the aluminum pad 4, and is used to increase the I/O bumping area. Then, a Ni layer or Ni-containing film is formed on the copper conductive lines 14, and used as the glue layer for the following bumping process. The photo resist layer is removed, and the upper portion of the Ti/Cu film 19 exposed by the remaining epoxy layer is removed.

Refer to Fig. 10, a second epoxy layer is coated on the copper conductive line 14, the Ni layer and the epoxy layer 10. The second epoxy layer is cured by UV curing or heating curing process to avoid the oxidation of the copper conductive line 14.

Referring to FIG. 11, a potion of the second epoxy layer 16 on the copper conductive lines 14 and Ni layer 17 is removed to form the third opening 15. The third opening 15 is above the copper conductive lines 14 and Ni layer 17, and the far

away form the external side of the copper conductive lines 14 (away from the aluminum pad 4) for the fan out type I/O structure.

Referring to FIG. 12, the solder ball 18 is bumped to the third opening 15 and on the Ni film 17 by a printing method. The solder ball 18 of the package structure is not located above the aluminum pad 4, but is extended to the lateral side of the metal pad 4.

A s shown in Fig. 13, the epoxy layer is cured by the IR reflow process. The wafer is transmitted to test the wafer level package, such as the final testing and sawing process. The dice are sawed with the scribe line 20 between the dice and the glass base 6 to separate the individual packaged structure.

The process of the present invention is more simple than the prior art. T he wafer level dice is tested before sawing, and the individual dice are formed by dividing along the scribed line and they are sucked and placed to form wafer level fan out type on the glass base.

Fig. 14 illustrates a diagram of the relationship among the Ni/Au or Ni-containing film, the Ti/Cu film or the Ni/Cu film, the Ni film 17, the glue layer and the barrier layer.

Fig. 15 illustrates a diagram of single wafer level fan out package. The capacitor 2b is introduced to the packaging process. Fig. 16 illustrates a cross-section diagram of the capacitor 2b bumped on the glass base and single dice of wafer level fan out package. In another embodiment, the multi dice or various passive elements can be integrated into the package process. Fig. 17 illustrates a cross-section diagram of the multi dice of the wafer level fan out package. The marks of 2a and 2c are defined as the different dice. The multi dice and various passive elements can be integrated into the package process to form the system in package by the process.

The characteristic of the present invention is the wafer level package, and the I/O

bumping positions on the dice are extended by the fan out process. The process can increases the I/O bumping numbers and avoid the signal interference caused by closer pitch.

The advantages of the present invention are as follows. 1. As shown in Fig. 1, the costs of the wafer level package are cheaper than the prior art. After selecting the tested and sawed dice, the processed dice are arranged on a new glass base to decrease the costs of the fan out type package. 2. The sizes of dice are scaled down due to minimization. The appropriate pitch between the dice is maintained (based on the requirement of the signal coupling). 3. The present invention can be applied to the package process of the 8-12 inches wafer. 4. The dice and the capacitor can be integrated to one package structure by the present invention. 5. The multi die or various passive elements can be integrated to one package structure, such as the CPU, DRAM, SRAM, by the present invention. 6. The solder of the epoxy layer is used as the buffer area. In following process, the problem of the imbalance stress generated by different materials can be avoided. 7. The base is glass and is same as the material of the dice base. Both of them have the same thermal coefficient of expansion (TCE) due to both material are composed with silicon. Therefore, the problem of the imbalance stress will not be generated. 8. The material of the base includes glass, ceramic, silicon to improve the reliability. 9. The costs on the new equipments are lower due to the available equipments are used. 10. The numbers of the solder balls can be improved, wherein some balls are used as the samples to output the dummy ball. Although absence of the capacity of signal transmission, the dummy ball can be used as the buffer zone to decreases the stress between different materials, and therefore, the problems of cracking can be avoided.

Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.

CLAIMS

What is claimed is:

1. A process of fan out type wafer level package, comprising the steps of:

providing a wafer having pluralities of dice formed thereon;

testing pluralities of said dice formed on said wafer and labeling good dice;

coating a BCB (Benzocyclobutene) isolating layer to protect said dice;

removing a portion of said BCB isolating layer and forming a first opening to expose the metal aluminum pad formed on said dice;

sawing said dice to separate said pluralities of dice;

selecting said processed dice and rearranging to attach on an isolating base by sucking and placing;

filling a first epoxy layer on said isolating base, said dice, said BCB and said aluminum pad of said first opening;

etching to remove said first epoxy layer above said aluminum pad, and forming a second openings;

curing said first epoxy layer;

sputtering a barrier layer on said aluminum pad;

soldering on said barrier layer by printing method and filling said second opening;

forming copper seed layer on solder and first epoxy layer;

electroplating certain region of copper conductive lines on said solder and said barrier layer by a photo resist;

forming Nickel-containing film or Aurum-containing film on said copper conductive lines;

removing said photo resist;

coating a second epoxy layer on said copper conductive lines;

curing said second epoxy layer;

removing portion of said second epoxy layer on said copper conductive lines and forming a third opening;

bumping solder balls to said third opening; and

sawing said isolating base to separate individual package unit.

2. The process in claim 1, further comprising sputtering a copper seed layer on said solder and said first epoxy layer before forming said copper conductive lines.

3. The process in claim 1, further comprising curing said glue layer during the step of attaching dice to said base.

4. The process in claim 1, wherein the thickness of said BCB isolating layer is approximately 5-25 μm.

5. The process in claim 1, wherein said step of etching said first epoxy layer to form said second opening is performed with photo resist or chemical reagent.

6. The process in claim 5, further comprising cleaning the surface of said dice by RIE plasma after forming said second opening.

7. The process in claim 1, wherein the materials of said barrier layer include Ni/Cu or Ni-containing film.

8. The process in claim 1, further comprising curing solder by an IR reflow method after said printing process.

9. The process in claim 2, wherein said copper seed layer include Ti/Cu.

10. The process in claim 1, wherein said step of curing said second epoxy layer comprising irradiating or heating by UV treatment.

11. The process in claim 1, wherein said step of bumping solder balls to said third opening is using printing process or bumping process.

12. The process in claim 1, further comprising a capacitor placed on the lateral side of said dice and arranged on said glass base.

13. The process in claim 1, further comprising another dice placed on the lateral side of said dice and arranged on said glass base to form multi dice package structure, said another dice include CPU, DRAM or SRAM.

14. The process in claim 1, wherein the material of said isolating base include glass.

15. The process in claim 1, wherein the material of said isolating base include ceramic.

16. The process in claim 1, wherein the material of said isolating base include silicon crystal.

17. A fan out type wafer level package structure, comprising:

an isolating base;

dice adhered to said isolating base, wherein said dice include pluralities of aluminum pad formed thereon;

BCB layer coated on the surface of said dice and having pluralities of first opening exposed to said pluralities of aluminum pad;

solder filled to said first opening;

a first epoxy layer coating on said dice, said isolating base and said BCB layer;

copper conductive lines placed to said first epoxy layer and connected with said solder;

a second epoxy layer coated on said copper conductive lines and having a second opening exposed a portion of said conductive lines; and

solder balls placed on said second epoxy layer and filling to said second opening and connected with said copper conductive lines.

18. The structure in claim 17, further comprising a copper seed layer formed on said first solder.

19. The structure in claim 18, wherein said copper seed layer include Ti/Cu.

20. The structure in claim 18, wherein said copper seed layer include Ni/Cu.

21. The structure in claim 17, further comprising a barrier or glue layer formed on said aluminum pad.

22. The structure in claim 21, wherein said barrier or glue layer include Ni/Al.

23. The structure in claim 17, wherein the interface of said solder balls and said copper conductive lines includes Ni.

24. The structure in claim 17, further comprising another capacitor placed on the lateral side of said dice.

25. The structure in claim 17, further comprising another dice placed on the lateral side of said dice.

Method for Fan Out Type Wafer Level Package

ABSTRACT

This invention relates to a package for semiconductors, and more particularly to a fan out type wafer level package. The present invention comprises sawing the dice, and the processed dice after selecting are adhered on the glass base. The I/O contact points of the metal pad on the dice fan out the contact points to the outside portion of the dice by the specific materials and processes. The process has larger area for I/O bumping. Therefore, the process can increase the I/O numbers and increase more I/O contact points, and decrease the signal coupling due to the too closer pitch and solder bridge due to the too closer contact points. The characteristic of the present invention includes the usage of the original machines, no additional costs, can be applied to the package process of the 8-12 inches wafer, and include the dice, the capacitor, the multi dice or various passive elements, such as the CPU, DRAM, SRAM. Besides, the material of the base is glass, and the present invention can avoid the problems of the imbalance stress due to the different material to improve the reliability.